UNIT-I: BASIC STRUCTURE OF COMPUTERS

1. With a neat diagram explain different processor registers (6M)      June 2010

2. Explain the important technological features and devices that characterized each
   generation of computers (6M)      Dec 2010

3. Discuss two ways in which byte addresses are assigned (8M)      June 2011

4. Explain the different functional units of a computer with a neat block diagram Dec 2011

5. Write the basic performance equation. explain the role of each of the parameters in
   the equation on the performance of the computer.      July 2012

UNIT-II- MACHINE INSTRUCTIONS AND PROGRAMS CONT'D.: 

1. What is an addressing mode .Explain different generic addressing modes with an
   example for each      June 2010

2. Define subroutine. Explain subroutine linkage using a link register      Dec 2010

3. Explain the shift and rotate operation with examples      June 2011

4. What is the need for an addressing mode? Explain the following addressing modes
   with examples: immediate, direct, indirect, index, relative      Dec 2011

5. a)What is subroutine linkage?how are parameters passed to subroutines      June 2012
   b. What is stack frame? Explain
UNIT-III- INPUT/OUTPUT ORGANIZATION

1. A. Explain the following (i) Interrupt concepts (ii) Interrupt hardware(5M)

B. Define exceptions. Explain two kinds of exceptions(7M)

c. What is the necessity of bus arbitration .Explain the different methods of bus arbitration.(4M)

d. Define the following(i) cycle stealing (ii) burst mode (4M)  June 2010

2. A. discuss the different schemes available to disable and enable the interrupts

B. how are simultaneous interrupt from more than one devices handled?

C. What does the term “cycle stealing” mean?

D. Write a short note on any 1 bus arbitration scheme.(10M)  Dec 2010

3. A. define and explain briefly the following(10M)

   i) Interrupt

   ii) Vectored in

   ii) Interrupt nesting

   An exception and give two examples

   B. Explain in with the help of a diagram the working of daisy chain with multiple priority levels and multiple devices in each level(10M)  June 2011

4. A. In modern computers, why interrupts are required ? Support your claim with suitable example (6)

   B. In the interrupt mechanism, how the simultaneous arrivals of interrupts from various (multiple) devices (I/O) are handled?(6)

   C. With neat sketches, Explain the various approaches to bus arbitration. (8) Dec 2011
5. A. Explain with a diagram, how interrupt request from several I/O devices can be communicated to a processor through a single INTR line (8)

   B. How can the processor obtain the starting address of different interrupt –service routines using vectored interrupts? (4)

   c. Why is bus arbitration required? Explain with block diagram bus arbitration using daisy chain. (8)

UNIT-IV- INPUT/OUTPUT ORGANIZATION CONTD.

1. A. Explain the important functions input/output interface(5M)

   B. With a neat block diagram explain a general 8-bit parallel interface circuit(8M)

   C. Explain the following w.r.t. USB(i) USB architecture (ii) USB addressing (iii) USB protocols(7M)

2. A. Draw and explain the block diagram of a typical serial interface. How does it compare with a parallel interface?(10M)

   B. explain the main phases involved in SCSI bus operation (10M)

3. A. in a computer system, PCI bus is used to connect devices to the processor (system bus) bus. Consider a bus transactional which the processor reads four 32-bit words from the memory. Explain the read operation on the PCI bus between memory and processor .give signal and timing diagram(10M)

   B. Draw the block diagram of universal bus(USB)structure connected to the host computer Briefly explain all fields of packets that are used for communication between a host and a device connected to an USB port.(10M)

4. A. With a neat sketch, explain the individual input and output interface circuits. Also elicit their salient feature. (10)

   B. in a computer system why a PCI bus is used? With a neat sketch, explain how the read
5. A. Explain with a block diagram a general 8 bit parallel interface. (8)

B. With the help of a data transfer signals explain how a real operation is performed using PCI bus. (8)

C. Explain briefly bus arbitration phase in SCSI bus. (4) June 2012

UNIT-V- MEMORY SYSTEM

1. A. with the block diagram, explain the operations of 16 megabit DRAM configured as 2Mx8 (6M)

B. Explain different mapping functions used in cache memory (8M)

C. What do you mean by memory interleaving? Explain.(6M) June 2010

2. A. differentiate between SRAM and DRAM(7M)

B. Sketch and explain the internal organization of a 2Mx8 dynamic memory chip(8M)

C. Explain any 1 cache mapping function. (5M) Dec 2010

3. A. Define and explain the following (4M)

   i) Memory access time
   ii) memory cycle time
   iii) Random access memory(RAM)
   iv) static memory

B. Differentiate the static RAM (SRAM) and dynamic RAM (DRAM) giving four key differences. State the primary usage of SRAM and DRAM in contemporary computer systems June 2011

C. Define memory latency and bandwidth in case of burst operation that is used for transferring a block of data to or from synchronous DRAM memory unit(8M)

4. A draw a diagram and explain the working of a 16-M bit DRAM chip configured as 2M x8
Also explain as to how it can be made to work in fast page mode (12M) Dec 2011

5. A. Draw the organization of a 1Kx1 memory cell and explain its working. (8)

   B. Explain the working of a single-transistor dynamic memory cell (7).

   C. Calculate the average access time experienced by a processor if a cache bit rate is 0.88, miss penalty is 0.015 milliseconds and cache access time is 10 microseconds.(5) June 2012

UNIT-VI: ARITHMETIC

1. A. what do you mean by address translation. Explain how TLB is used to implement virtual memory(6M)

   B. Mention four major functions of disk controller on disk drive side.(7M)

   C. Explain how a 16-bit carry look ahead adder can be built from 4-bit adder (7M) Dec 2009

2. A. Draw a block diagram and explain how a virtual address from the processor is translated into a physical address in the main memory(6M)

   B. write short notes on (i) optical technology used in CD systems (ii) RAID disk arrays(8M)

   C. Draw a figure to illustrate and explain a 16-bit carry look ahead adder using 4-bit adder blocks. Show that the sum and carry are generated in 5 and 8 gate delays respectively(6M)

       June 2010

3 .A. Explain a simple method of translating virtual address of a program into physical address, with the help of a diagram (8)

   B. Explain structural organization of moving head magnetic hard disk, with multiple surfaces for storage of data. Explain hw moving head assembly works for reading data(6M) Dec 2010

   C. Answer the following w.r.t. to magnetic disk, the secondary storage device(6M)

   i) Seek time
ii) Latency

iii) Access time

4. Explain in detail the working principle of a magnetic hard disk(10) Dec 2011

5. A. Show the organization of virtual memory address translation based in fixed-length pages and explains its working. (8)

B. How can performance and reality be improved using RAID technology? (4)

C. Explain the design of a 4-bit carry-look-a-head adder. (8) June 2012

UNIT-VII: BASIC PROCESSING UNIT

1. A. Show the multiplication of (+13) and (-6) using multiplier bit pair recording technique. (6M)

B. Differentiate between restoring and non restoring division(6M).

C. Explain the IEEE standard for floating point number representation.(8M) June 2010

2. A. Draw the hardware implementation of Booth’s multiplication algorithm.(7M)

B. Trace the steps in the above implementation to multiply -5x-4(7M)

C. Illustrate the steps for non restoring division algorithm on the following data:

<table>
<thead>
<tr>
<th>dividend</th>
<th>divisor</th>
<th>quotient</th>
</tr>
</thead>
<tbody>
<tr>
<td>1011</td>
<td>0101</td>
<td></td>
</tr>
<tr>
<td>Dec 2010</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3. A In carry look a head addition explain generating G_i and propagating P_i functions for stage I with the help of Boolean expression for G_i and P (12M)

B. Performance signed multiplication of numbers -12 and -11 using both multiplication algorithm represent the numbers in 5-bit including sign bit .Give booth multiplier recording table that is used in the above multiplication(8)

C. Perform division of numbers 8 by 3 using non-restoring division algorithms (8) June 2011

4. A. Draw circuit diagram for binary division .explain the restoring and non restoring division
algorithm with suitable examples (12M)

B. Explain the concept of carry save addition for the multiplication operation, \( M \times Q = P \) for 4-bit operands, with diagram and suitable examples (8M)  

Dec 2011

5. A. Explain Booth’s algorithm Multiply 01110 (+14) and 11011 (-5) using Booth’s multiplication (10)

B. Write the algorithm for binary division using restoring division method (4)

C. List the rules for addition, subtraction, multiplication and division of floating point numbers (6)  

June 2012

UNIT-VIII: MULTICORES, MULTIPROCESSORS, AND CLUSTERS

1. A. Write and explain the control sequences for execution of following instruction

   \( \text{Add}(R3),R1 \) (6M)

B. With neat diagram, explain 3 bus organization and write control sequence for the instruction

   \( \text{Add} \ R1,R2,R3 \). (7M)

C. Differentiate between hardwired and micro programmed control (7M)  

June 2010

2. A. Draw a figure of single bus organization of the processor unit (6M)

B. List the actions needed to execute the instruction \( \text{Add} \ R1,(R3) \). Write the sequence of control steps to perform actions for a single bus structure. Explain the steps (8M)

C. Compare hardwired control unit with micro programmed control unit (6M)  

Dec 2010

3. A. Draw the block diagram of the three-bus organization of data path, which provides multiple internal paths to enable several transfers to take place in parallel. Label the registers and functional components of the processor and their connection to respective bus of data path (16)

B. Draw a block of a complete processor and identify the units (4)  

June 2011

4. A. Explain the process of fetching a word from memory using timing diagram of memory read operation. Also give an example for the same (12)  

Dec 2011
5. A. Write and explain the control sequences for the execution of an unconditional branch instruction (10)

B. Explain with block diagram the basic organization of a microprogrammed control unit (8)

C. What are modifications required in the basic organization of a microprogrammed control unit to support conditional branching in the microprogram (2)